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(73) Proprietor: **SONY CORPORATION**
7-35 Kitashinagawa 6-chome
Shinagawa-ku
Tokyo 141(JP)

(72) Inventor: **Yamamoto, Yoshihiro**
c/o Sony Corporation
7-35 Kitashinagawa 6-chome
Shinagawa-ku Tokyo(JP)
Inventor: **Kume, Tsutomu**
c/o Sony Corporation
7-35 Kitashinagawa 6-chome
Shinagawa-ku Tokyo(JP)
Inventor: **Yamazaki, Nobuo**
c/o Sony Corporation
7-35 Kitashinagawa 6-chome
Shinagawa-ku Tokyo(JP)
Inventor: **Hashimoto, Fumiharu**
c/o Sony Corporation
7-35 Kitashinagawa 6-chome
Shinagawa-ku Tokyo(JP)
Inventor: **Ohya, Koichi**
c/o Sony Corporation
7-35 Kitashinagawa 6-chome
Shinagawa-ku Tokyo(JP)

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(74) Representative: **Schmidt-Evers, Jürgen, Dipl.-Ing. et al**
Patentanwälte Mitscherlich & Partner,
Sonnenstrasse 33,
Postfach 33 06 09
D-80066 München (DE)

Description

Field of the Invention

This invention relates to a filter circuit and, more particularly, to a so-called double integration type filter circuit consisting essentially of a pair of integrators connected in series with each other.

Description of the Prior Art

In general, in a process of checking an electronic circuit, it may become necessary to adjust the peak frequency, dip frequency or the cut-off frequency of the filter circuit to a prescribed target value. Above all, in a circuit formed in an analog IC, the circuit elements such as transistors, resistors or capacitors may be fabricated with a rather accurate relative ratio of the rated values thereof, but the magnitudes of these rated values usually vary from circuit to circuit. Hence, the aforementioned adjustment is thought to be indispensable in view of a demand for higher accuracy in the filter circuit.

The EP-A-0 012 876 describes a double integragtion type band pass filter circuit. The centre frequency of the filter can be adjusted without significant change of the value of Q by variation of a resistor. During adjustment, the filter configuration the centre frequency of which is equal to the target frequency is fixed.

It is noted herein that a double integration type filter circuit as disclosed, for example, in the United States Patent No. 4,472,689, can be built into an IC. The double integration type filter circuit has advantages that a higher accuracy suitable for incorporation into an IC may be realized and that it allows various filter characteristics, including the value of Q_1 to be adjusted more easily.

It is noted that, at the time of adjusting the filter circuit, it has so far been necessary to detect portions proper to the characteristic curves, such as so-called cut-off points or peak portions, and to adjust the frequencies of these portions, namely the so-called cut-off or peak frequencies, to prescribed target values. However, it is troublesome or even difficult with the LPF, HPF or the BFP with its low value of Q to locate the cut-off or peak points accurately on the characteristic curves.

Above all, when it is desired to automate such filter adjustment, it is difficult to discriminate and read out mechanically those characteristic portions, such as the aforementioned cut-off points, from the frequency characteristic curves, thus occasionally resulting in lowered adjustment accuracy.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention according to Claim 1 to provide a filter circuit wherein the portions proper to the filter characteristics can be detected easily and accurately during the filter adjustment.

It is another object of the present invention to provide a filter circuit so designed that the characteristics can be detected easily and accurately during the filter adjustment.

It is another object of the present invention to provide a filter circuit so designed that the characteristics thereof can be adjusted highly accurately and within a reduced adjustment time.

According to the present invention, there is provided a filter circuit comprising a pair of integrators each consisting of an amplifier and an integration capacitance, with the output terminal of the first integrator being connected to the input terminal of the second integrator and with the output terminal of the second integrator being connected to the input terminal of the first integrator and to the input terminal of the said second integrator, wherein an improvement resides in that a changeover switch is provided for commutation of filter characteristics, said changeover switch being commutated during the filter adjustment for providing a filter configuration which will allow for better recognition of the portions proper to filter characteristics.

With the above described filter circuit, the circuit is commutated to a specific filter configuration, such as a trap filter configuration, that allows those portions proper to the filter characteristics to be recognized more easily, or the Q of the filter is increased to provide the characteristics placing an emphasis on the shape of the cut-off, dip or peak portions. In this manner, filter adjustment can be made more easily and accurately.

According to a preferred embodiment of the present invention, optimum adjustment data are obtained on the basis of filter adjustment data associated with the point of intersection of the filter output level with a reference level, while the filter characteristics are changed during application of a constant frequency input signal, so that the adjustment may be completed within a shorter time with a higher adjustment accuracy despite the simplified circuit constitution, and the circuit may be adapted more easily to automation of filter adjustment operations.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block circuit diagram showing a filter circuit according to an embodiment of the present invention.

Fig. 2 is a chart for explaining the operation of commutating the characteristics of the filter circuit shown in Fig. 1.

Fig. 3 is a circuit diagram showing a practical example of an integrator employed in the filter circuit of Fig. 1.

Fig. 4 is a block circuit diagram showing an analog IC and a filter adjustment system to which the above embodiment is applied.

Fig. 5 is a chart for explaining the adjustment of the frequency characteristics of the trap filter.

Fig. 6 is a chart for explaining a practical example of the operation of adjustment of the trap filter.

Fig. 7 is a block circuit diagram showing a modified embodiment of the present invention.

Fig. 8 is a chart for explaining the characteristics of the filter circuit of Fig. 7.

Fig. 9 is a block circuit diagram showing another modified embodiment of the present invention.

Fig. 10 is a chart for explaining the operation of the filter circuit of Fig. 9.

Fig. 11 is a block circuit diagram showing still another embodiment of the present invention.

Fig. 12 is a chart for explaining the operation of the filter circuit of Fig. 11.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Fig. 1 is a block circuit diagram showing a filter circuit according to an embodiment of the present invention, and illustrates a so-called biquad filter of the double integration type built into an associated IC. In this figure, a low pass filter LPF is shown, wherein the connection of various circuit portions is commutated and changed, only when the filter adjustment is required, to a filter circuit configuration whose filter characteristics are suitable for filter adjustment and can be detected easily, such as a trap filter circuit configuration, said connection being restored to the original LPF after termination of adjustment.

The biquad filter shown in Fig. 1 is a so-called active filter comprised of a series circuit of a first integrator composed of a first operational amplifier 11 and a first integration capacitance or capacitor 12 and a second integration composed of a second operational amplifier 13 and a second capacitor 14. The output of the operational amplifier 11 is supplied to a non-inverting input terminal of the operational amplifier 13 while the output of the operational amplifier 13 is fed back to an inverting input terminal of the operational amplifier 11 and the output of the operational amplifier 13 is also fed back to a non-inverting input terminal of the operational amplifier 13 via a feedback circuit 15 having a feedback factor β. The feedback circuit 15 is composed of a voltage divider composed of resistors R_1 and R_2, with the resistor R_2 being connected to an output terminal of the operational amplifier 13. With the above described arrangement of the double integration type biquad filter, the characteristics of FPF, LPF, HPF, trap or a phase shifter may be realized depending on various combinations of the non-inverting input terminal Ta of the operational amplifier 11, the terminal Tb, i.e. the junction point with the resistor R_1, of the capacitor 12 as the integration capacitance, and the terminal Tc of the capacitor 14, being supplied with input signals or grounded. The Table 1 below shows various filter characteristics that may be realized depending on the selection as to supplying the input signals or grounding these terminals Ta, Tb or Tc.

TABLE 1

	Ta	Tb	Tc
LPF	supplied with input signals	grounded	grounded
BPF	grounded	supplied with input signals	grounded
HPF	grounded	grounded	supplied with input signals
trap	supplied with input signals	grounded	supplied with input signals

In the embodiment shown in Fig. 1, input signals are supplied to the non-inverting input terminal Ta of the operational amplifier 11 from a signal source SG through an input terminal 16, while the other terminal of the capacitor 12, i.e. the junction point of the capacitor 12 with the resistor R_1, is grounded. The other terminal Tc of the capacitor 14 is connected to a changeover switch 18 so that the aforementioned input

signals may be supplied therethrough to the terminal Tc or the terminal Tc may be grounded through selective commutation of the changeover switch 18. In this manner, selection may be made between the trap filter for the intended ajustment of the filter characteristics and the LPF as the intrinsic filter. Thus the input terminal 16 is connected to a select terminal a of the changeover switch 18, while a select terminal b is grounded. The output signals are taken at an output terminal 17 of the operational amplifier 13. The frequency characteristics of the trap filter with the changeover switch 18 being connected to the selected terminal a may be represented by a transfer function.

$$\frac{s^2 + 1}{s^2 + \beta s + 1}$$

where

$$S = j \frac{\omega}{\omega_0},$$

$\omega_0 = 2\pi fo$, $\omega = 2\pi f$ and f_0 is the trap frequency of the trap filter whereas those of the LPF, realized with the changeover switch 18 being connected to the select terminal b, are represented by the transfer function

$$\frac{1}{s^2 + \beta s + 1}$$

wherein

$$s = j \frac{\omega}{\omega_0},$$

$\omega_0 = 2\pi fo$, $\omega = 2\pi f$ and f_0 is the cut-off frequency of the low pass filter.

Hence, during normal usage of the circuit shown in Fig. 1, the changeover switch 18 is leveled to the terminal b in order to realize the LPF having frequency characteristics shown by the solid line in Fig. 2. During the filter adjustment, the changeover switch 18 is leveled to the terminal a in order to realize trap filter characteristics as indicated by the chain-dotted line in Fig. 2. The output level of the output signals from the output terminal 17 is measured by a level measurement device LM, such as a level meter, for detecting the dip portion proper to the filter characteristics, and the filter adjustment is made until the dip frequency f_0 coincides with the prescribed target frequency. In this manner, filter adjustment can be made by using filter characteristics, such as the dip portion of the trap characteristics, that can be detected more easily than, for example, the cut-off point of the LPF, so that filter adjustment can be achieved more easily and accurately.

Fig. 3 shows an example of an integrator used in the above biquad filter. Referring to Fig. 3, the non-inverting input terminal 21 and the inverting input terminal 22 of the operational amplifier 11, 13 of Fig. 2 are connected to the base terminals of transistors 23, 24 cojointly forming a differential amplifier. The current flows in a resistor R_E connected between the emitters of these transistors 23, 24 with the magnitude of the current being related to the input voltage between the terminals 21 and 22. The current equal to the sum of the currents I_1, I_1 of the constant current sources connected to the emitters of the transistors 23, 24 and the current equal to the difference between the currents I_1, I_1 flow respectively through diodes 25, 26 connected to the collectors of the transistors 23, 24, respectively. The terminal voltages of these diodes 25, 26 appearing as a function of these currents are applied to the base electrodes of transistors 27, 28 cojointly forming an emitter common differential transistor pair. The common emitter of these transistors 27, 28 is grounded via a constant source 29 of the currents $2I_2$, such that the signal current flowing at the collector side of the differential transistor pair is amplified by a factor if I_2/I_1. The collector output of the

transistor 28 is taken through a current mirror circuit 30 for charging the capacitor 32 used as the aforementioned integration capacitance. The voltage at one terminal of the capacitor 32 is inputted to a transistor 34 so as to be taken at an output terminal 35. The other terminal 33 of the capacitor 32 is grounded or alternatively an input signal is supplied thereto, as mentioned hereinabove.

In the integrated circuit configuration shown in Fig. 3, by changing the current I_2 of the current source 31 on the output side of the current mirror circuit 30 and the constant current source 29, the frequency characteristics of the biquad filter of Fig. 1, more specifically, the trap filter characteristic curve or the low pass filter characteristic curve of Fig. 2, are shifted in the direction parallel to the frequency axis, for adjustment of the cut-off or dip frequencies. At the time of the actual filter adjustment, the changeover switch 18 is leveled to the terminal a for changing the filter characteristics to those of a trap filter for easiness in the detection of those portions proper to the filter characteristic curve.

Referring to Fig. 4, there is shown an embodiment in which the filter circuit of the preceding embodiment is included within an analog IC, such as sound multiplex demodulating IC, employed in, for example, a television receiver. The filter 2 provided in the analog IC 1 of the Fig. 4 corresponds to the biquad filter circuit shown in Fig. 1. It is the frequency characteristics of the filter 2 that are to be adjusted.

Referring to Fig. 4, signals of a constant frequency f_0 are supplied from a signal source SG to the filter 2 through an external connection terminal or pin of the analog integrating circuit IC 1. It is noted that the circuit constants of the filter 2, such as the current I_2 in the constant current sources 29 and 31, are changed as a function of the filter adjustment data for changing the filter characteristics. The filter 2 shows LPF characteristics, as indicated by the solid line in Fig. 2, during the normal usage thereof. It also shows trap filter characteristics as indicated by the chain-dotted line therein only during the time of filter adjustment. It is noted that the signal frequency f_0 from the signal source SG is set so as to be equal to the target adjustment value of the cut-off frequency of the 49F and the dip frequency of the trap filter. Thus, in the present embodiment, filter adjustment is performed so that the cut-off frequency of the dip frequency at the time of filter adjustment will be ultimately equal to the aforementioned constant frequency f_0.

The output from the filter 2 is supplied to a level detector 5, such as the so-called AM detector, previously provided in the analog IC 1, for detecting the signal level or amplitude, with the detected level output being supplied to one input terminal, such as the non-inverting input terminal, of the comparator 6, for level discrimination. To the other input terminal, such as the inverting input terminal, of the comparator 6, there is supplied a prescribed reference level V_{ref} through a reference input terminal 7. The comparator 6 discriminated whether the detected output level is higher or lower than the reference level V_{ref}. The output from the comparator 6 or the discriminated level output is supplied to an internal bus 40 in the IC 1. A bus decoder 41 connected to the internal bus 40 of the IC 1 is also connected to an external bus 50 through a terminal for external connection 42 so as to be used as an interfacing circuit for exchange of data on the external bus 50 and those on the internal bus 40. The data transmitted from the external bus 50 through the bus decoder 41 to the internal bus 40 are stored in a latch circuit 43 so as to be then converted in a DA converter 44 into analog signals which are supplied to the filter 2 as the circuit constant control signals or as the filter adjustment signals. To the external bus 50, there are connected a CPU 51 such as the microprocessor, a ROM 52 where the programs or data are written in advance, a RAM 53 where data, etc. are written transiently, and a non-volatile memory 54 where filter adjustment data, etc. as later described may be stored positively no mater whether the power source is turned on or off. The computer system mainly composed of the CPU 51, ROM 52, RAM 53 and the non-volatile memory 54, performs a series of control operations, such as commutation of the changeover switch in the filter 2, setting of the filter characteristics and the selection of the optimum filter adjustment data based or the output from the comparator 6 that is changed with changes in the filter adjustment data.

The operation of finding these optimum filter adjustment data is now explained.

In general, when making the filter adjustment, the aforementioned dip frequency may be detected on the basis of the filter output characteristic curve or the frequency response curve that is obtained when changing or sweeping the input signal frequency with the frequency sweeping being repeated until the dip frequency is equal to the target frequency f_0, while the filter characteristics are adjusted, as conventionally. There is, however, proposed in the present embodiment, a system as shown in Fig. 4 wherein filter adjustment can be made automatically and precisely by a circuit of a simpler constitution.

Briefly, the filter adjustment system is so designed that the optimum filter adjustment data are obtained on the basis of those data corresponding to the crossing of the prescribed reference level by the level detection filter output, while the filter characteristics are changed with the input signal being fixed at the constant frequency f_0.

Thus, during filter adjustment, the changeover switch 18 in the filter 2 is commutated to the select terminal a by switch commutation data from control means consisting mainly of the CPU 21, in such a

manner that the characteristics of the filter 2 are commutated to the aforementioned trap characteristics. Fig. 5 illustrates a characteristic curve of a trap filter obtained upon the aforementioned filter adjustment. The filter characteristics are adjusted so that the frequency of the dip in the characteristic curve of the trap filter will be equal to a prescribed target frequency f_0.

It will be noted herein that signals of a constant frequency f_0 are supplied from the signal source SG to the filter 2. At this time, filter adjustment data are supplied by a control means consisting of a computer system including the CPU 51 to current control terminals of the constant current sources 29, 31 of the aforementioned integrator in the filter 2 through the bus decoder 11, internal bus 10 in the IC, latch circuits 43A and 43B and the AD converter 44. These adjustment data represent a series of data for gradually shifting the characteristic curves of the filter 2B in one direction, for example, in the direction shown by the arrow mark in the figure, as schematically indicated therein, on the frequency axis. It is noted that changing the frequency characteristics in this manner substantially continuously is tantamount to changing or sweeping the input signal frequency according to the prior art practice.

Conversely, since the input signal frequency is fixed at the constant value f_0, the output obtained after level detection of the output signals from the filter 2 at the AM detector 5 is as shown, for example, at the detected output in Fig. 6. The detected output has its level changed in accordance with the changes in the filter adjustment data as indicated on the abcissa in Fig. 4. Thus, the curve of the detected output corresponds to the filter characteristic curve of Fig. 3 supposed to be inverted in the left and right direction in Fig. 3 with the frequency f_0 as the center. This detected output is supplied to the non-inverting input terminal of the comparator 6 for comparison with the reference level V_{ref} to produce the comparator output as shown in Fig. 6. When assumed that the filter adjustment data obtained at the inverting position of the comparator output, that is, when the detected output intersects the reference level V_{ref}, are sequentially denoted as Da and Db, the optimum adjustment data, that is, the data for the time when the dip frequency of the trap frequency coincides with the aforementioned frequency f_0 is obtained from the mean value of the data Da and Db or (Da + Db)/2. These optimum adjustment data are written in the non-volatile memory 54 of Fig. 4 and there stored even when the power source is turned off. As one of the initializing operations usually performed at the time the power source is turned on, the aforementioned optimum adjustment data stored in the non-volatile memory 54 is transmitted to the latch circuit 43 through the buses 50 and 40 for establishing the optimum adjustment state for the filter 2.

It is possible with the above arrangement to eliminate the conventional frequency sweeping, while simplifying the circuit structure and shortening the time otherwise necessary for adjustment. In addition it is possible to obtain the optimum filter adjustment data with high accuracy by a simpler structure comprising a comparator 6 adapted for detecting the crossing point of the reference level by the filter output, with the monitoring of the characteristic curve being also eliminated, while the circuit can be easily adapted to automatic adjustment with the use of buses.

The present invention is not limited to the above embodiment but may also be applied to, for example, an adjustment of the cut-off frequency of a BPF. Referring now to Fig. 7, changeover switches 18A, 18B are operatively interlocked with each other, while the non-inverting terminal Ta of the operational amplifier 11 and the other terminal Tc of the capacitor 14 of the second integration capacitance are connected in common to a common terminal of the changeover switch 18A. The other terminal Ta of the capacitor 12 as the second integration capacitance is connected to a common terminal of the changeover switch 18B while the select terminal b of the changeover switch 18A and the select terminal a of the changeover switch 18B are connected in common to a signal input terminal 16, while the select terminal a of the changeover switch 18A and the select terminal b of the changeover switch 18B are connected in common and grounded. The circuit design is otherwise the same as that of Fig. 1 so that the same or equivalent parts are denoted by the same reference numerals and the corresponding description is omitted for simplicity.

With the arrangement of Fig. 7, both the changeover switches 18A, 18B are connected to the select terminal a, during the normal usage of the circuit, for constituting the BPF having the frequency characteristics shown by the solid line in Fig. 8. The changeover switches 18A, 18B are connected to the select terminal b of the changeover switches 18A, 18B during filter adjustment for commutation to the trap filter characteristics as indicated by the chain dotted line in Fig. 8 similarly to the embodiment of Fig. 1. In this manner, the portion proper to the characteristic curve may be demonstrated in the form of a dip that may be detected easily to permit filter adjustment to be conducted more easily and with improved accuracy.

Fig. 9 shows in a block circuit diagram the filter circuit according to a further modification of the present invention and illustrates the so-called biquad filter of the double integration type that is build into an IC. In the present embodiment, the value of Q in, for example, a BPF, is enlarged only during filter adjustment to increase the sharpness of the peak portion proper to the filter characteristics to facilitate the detection of the

frequency of the peak portion and hence to facilitate the filter adjustment.

The biquad filter shown in Fig. 9 is a so-called active filter consisting of a series circuit of a first integrator composed of a first operational amplifier 11 and a capacitor as integration capacitance 12 and a second integrator composed of a second operational amplifier 13 and a second capacitor 14. The output of the operational amplifier 11 is supplied to a non-inverting terminal of the operational amplifier 13, the output of the operational amplifier 13 is fed back to an inverting input terminal of the operational amplifier 11, and the output of the operational amplifier 13 is fed back to the inverting input terminal of the operational amplifier 13 through a feedback circuit 15 having a feedback factor β. The feed back circuit 15 is composed of a voltage divider consisting of resistors R_1 and R_2, with the resistor R_2 being connected to the output terminal of the operational amplifier 13.

As essential portions of the present embodiment, a series circuit consisting of a resistor R_3 and a switch SW is connected parallel to the resistor R_1. The feedback factor β of the feedback circuit 15 is commutated by the turning on and off of the switch SW for commutating only the value of Q of the filter.

It will be noted herein that a variety of filter characteristics such as those of a BPF, LPF, HPF or a trap filter may be achieved according as the non-inverting input terminal of the operational amplifier 11 or the capacitors 12, 14 are fed with input signals or grounded. In the emobidment shown in Fig. 9, both the non-inverting terminal of the operational amplifier 11 and the capacitor 14 are grounded, while the input signals are supplied from the signal source SG to the capacitor 12 and to a resistor R_1 of the feedback circuit 15 through the input terminal 16 for constituting the BPF. The frequency characteristics of the BPF are represented by the transfer function

$$\frac{\beta}{s^2 + \beta s + 1}$$

wherein $S = j\omega/\omega_o$, $\omega_o = 2\pi fo$, $\omega = 2\pi f$ and f_0 is the cut-off frequency of the band pass filter.

It is noted that, in the circuit configuration shown in Fig. 9, the feedback factor β in the feedback circuit 15 is commutated in accordance with the turning on and off of the switch SW in the feedback circuit 15, such that the feedback factor β_{OFF} during the time the switch SW is turned off is given by

$$\beta_{OFF} = \frac{R_1}{R_1 + R_2}$$

while the feedback factor β_{ON} during the time the switch SW is turned on is given by

$$\beta_{ON} = \frac{R_1 // R_3}{(R_1 // R_3) + R_2}$$

wherein

$$R_1 // R_3 = \frac{R_1 R_3}{R_1 + R_3}.$$

As to the values of Q for these states Q_{OFF} and Q_{ON}, $Q_{OFF} = 1/\beta_{OFF}$ and $Q_{ON} = 1/\beta_{ON}$, so that $Q_{OFF} < Q_{ON}$.

Thus, during the normal usage of the circuit, the switch SW is turned off to realize the BPF having the frequency characteristics as indicated by the solid line in Fig. 10. During filter adjustment, the switch SW is turned on for commutating the filter characteristics to those of a BPF having a larger value of Q as indicates by the double-dotted chain line in Fig. 10, while the level of the output signal from the output terminal 17 is measured by a level measuring device, such as a level meter, for detecting the peak portion proper to the characteristic curve, and the filter adjustment is performed until the peak frequency f_0 is coincident with the

prescribed target frequency. In this manner, adjustment of the BPF can be made easily and accurately by increasing the value of Q for enhancing the sharpness of the peak portion only during the adjustment, despite the fact that the value of Q of the BPF is low and hence it is difficult to identify its peak frequency as may be seen from the frequency characteristics as indicated by the solid line in Fig. 10.

It can also be applied to adjustment of the cut-off frequency of a low pass filter to increase the value of Q of the filter. In this case, input signals are supplied to a non-inverting input terminal of the operational amplifier 11 of the first integrator through the input terminal 16, while both the capacitors 12, 14 of the integration capacitances of the first and second integrators and the resistor R_1 of the feedback circuit 15 are grounded, for constituting the LPF, a series circuit consisting of the resistor R_3 and the switch SW is connected in parallel with the resistor R_1, this switch SW being turned on and off to commutate the value of Q. Thus, during normal usage of the circuit, the switch SW is turned off to realize the LPF characteristics as indicated by the solid line in Fig. 12. During filter adjustment, the switch SW is turned on to elevate the value of Q to produce a peak in the vicinity of the cut-off frequency f_0 of the characteristic curve of the LPF as indicated by the double-dotted chain line in Fig. 12 for facilitating the detection of the cut-off frequency f_0. The circuit design is otherwise the same as that shown in Fig. 9 so that the same or equivalent parts are indicated by the same reference numerals and the corresponding description is omitted for simplicity.

Claims

1. A filter circuit comprising:

a pair of integrators (11, 12; 13, 14) each having an amplifier (11; 13) and an integration capacitance (12; 14), with an output terminal of the first one of said integrators (11, 12) being connected to an input terminal of a second one of said integrators (13, 14), with an output terminal of said second integrator (13, 14) being fed back to an inverting input terminal of said first integrator (11, 12) and to an inverting input terminal of said second integrator (13, 14) via a feedback circuit (15) and with the integration capacitance (12) of said first integrator (11, 12) being connected to said feedback circuit (15);

switch means(18; SW, 15) connected to at least one of said first and second integrators (11, 12; 13, 14) for commutating the characteristics of said filter circuit; and

means responsive to a control signal for selectively operating said switch means (18; SW, 15);

characterized in

that the output terminal of said first integrator (11,12) is connected to the non-inverting input of said second integrator (13, 14);

that the non-inverting input terminal (Ta) of the first integrator (11, 12), the junction point (Tb) of said integration capacitance (12) of said first integrator with said feedback circuit (15) and a terminal (Tc) of the integration capacitance (14) of the second integrator (13, 14) are supplied with input signals or grounded, respectively, for selectively forming different filter configurations; and

that said switch means (18; SW, 15) is adapted for commutating the filter circuit from a first filter configuration to a second filter configuration during adjustment, said second filter configuration having a filter characteristics being more distinct and thus more suitable for easy and accurate adjustment than the filter characteristics of said first filter configuration.

2. A filter circuit according to claim 1, characterized by means responsive to a second control signal for adjusting the characteristics of said filter circuit while said switch means (18, SW, 15) is operated.

3. A filter circuit according to claim 1 or 2, characterized in that said switch means includes a switch unit (SW) for commutating the value of Q of said filter circuit, said switch unit (SW) being commutated for increasing the value of Q, during adjustment of said filter circuit.

4. A filter circuit according to any one of claims 1 to 3, characterized by input supplying means (16, SG) for supplying a constant frequency input signal to one of said integrators (11, 12; 13, 14).

5. A filter circuit according to claim 4, characterized in that the output terminal of the integration capacitance (12) of said first integrator (11, 12) is connected to a ground terminal, and characterized by means for connecting the inverting input terminal of said second integrator (13, 14) to a ground terminal, said input supplying means connecting the non-inverting input terminal of said first integrator (11, 12) to receive said constant frequency input signal, said switch means (18) is adapted for selectively connecting the output terminal of the integration capacitance (14) of said second integrator

(13, 14) to the non-inverting input terminal of said first integrator (11, 12) or to said ground terminal.

6. A filter circuit according to claim 4, characterized in that the inverting input terminal of said second integrator (13, 14) is connected to the integration capacitance (12) of said first integrator (11, 12), said switch means (18) is comprised of a first switch unit (18A) adapted for selectively connecting the non-inverting input terminal of said first integrator (11, 12) to said ground terminal or to said constant frequency input signal, and a second switch unit (18B) for selectively connecting the integration capacitance (12) of said first integrator (11, 12) to said ground terminal or to said constant frequency input signal, said first and second switch units (18A, 18B) being operated while said switch means (18) is operated to connect said constant frequency input signals to the non-inverting input of said first integrator (11, 12) and to connect the integration capacitance (12) of the first integrator (11, 12) to ground.

7. A filter circuit according to claim 4, characterized in that the integration capacitance (12) of said first integrator (11, 12) is connected to said constant frequency input signal, said switch means (15) including a resistor circuit (R_1, R_2, R_3) connected to the output terminal and to the inverting input terminal of said second integrator (13, 14) and to the integration capacitance (12) of said first integrator, said switch unit (SW) commutating the value of resistance of said resistor circuit (R_1, R_2, R_3).

8. A filter circuit according to claim 4, characterized in that the non-inverting input terminal of said first integrator (11, 12) is connected to said constant frequency input signal, and said switch means (15) includes a resistor circuit (R_1, R_2, R_3) connected to the output terminal of said second integrator (13, 14) and to ground, said switch unit (15) commutating the value of resistance of said resistor circuit (R_1, R_2, R_3).

9. A filter circuit according to any one of claims 1 to 8, characterized in that said switch means (18, 15, SW) is operated for commutating the filter characteristics of said filter from a low pass filter to a trap type filter during adjustment of said filter circuit.

10. A filter circuit according to any one of claims 1 to 8, characterized in that said switch means (18, 15, SW) is operated for commutating the filter characteristics of said filter from a bandpass filter to a trap type filter during adjustment of said filter circuit.

Patentansprüche

1. Filterschaltung, die umfaßt:

zwei Integrierer (11,12;13,14), wobei jeder einen Verstärker (11;13) und eine Integrierkapazität (12;14) hat, mit einem Ausgangsanschluß des ersten der Integrierer (11,12), der mit dem Eingangsanschluß des zweiten der Integrierer (13,14) verbunden ist, mit einem Ausgangsanschluß des zweiten Integrierers (13,14), der zu einem invertierenden Eingangsanschluß des ersten Integrierers (11,12) und zu einem invertierenden Eingangsanschluß des zweiten Integrierers (13,14) über eine Rückkopplungsschaltung (15) zurückgeführt ist, und mit einer Integrierkapazität (12) des ersten Integrierers (11,12), die mit der Rückkopplungsschaltung (15) verbunden ist;

Schaltmittel (18;SW,15), die mit wenigstens einem der ersten und zweiten Integrierer (11,12;13,14) verbunden sind, um die Charakteristik der Filterschaltung umzuschalten; und

Mittel, die auf ein Steuersignal antworten, um wahlweise die Schaltmittel (18;SW,15) zu betätigen;

dadurch gekennzeichnet,

daß der Ausgangsanschluß des ersten Integrierers (11,12) mit dem nichtinvertierenden Eingang des zweiten Integrierers (13,14) verbunden ist;

daß der nichtinvertierende Eingangsanschluß (Ta) des ersten Integrierers (11,12), der Verbindungspunkt (Tb) der Integrierkapazität (12) des ersten Integrierers mit der Rückkopplungsschaltung (15) und ein Anschluß (T_c) der Integrierkapazität (14) des zweiten Integrierers (13,14) jeweils mit Eingangssignalen beliefert oder geerdet werden, um wahlweise verschiedene Filterkonfigurationen zu bilden; und

daß die Schaltmittel (18;SW,15) angepaßt sind, um die Filterschaltung von einer ersten Filterkonfiguration zu einer zweiten Filterkonfiguration während einer Justierung umzuschalten, wobei die zweite Filterkonfiguration eine Filtercharakteristik hat, die für eine leichte und genaue Justierung ausgeprägter und folglich geeigneter ist als die Filtercharakteristik der ersten Filterkonfiguration.

2. Filterschaltung nach Anspruch 1, gekennzeichnet durch Mittel, die auf ein zweites Steuersignal antworten, um die Charakteristik der Filterschaltung zu justieren, während die Schaltmittel (18,SW,15) betätigt sind.

3. Filterschaltung nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die Schaltmittel eine Schalteinheit (SW) umfassen, um den Q-Wert der Filterschaltung umzuschalten, wobei die Schalteinheit (SW) umgeschaltet wird, um den Q-Wert während einer Justierung der Filterschaltung zu erhöhen.

4. Filterschaltung nach einem der Ansprüche 1 bis 3, gekennzeichnet durch Eingangssignalliefermittel (16,SG), um ein Eingangssignal mit einer konstanten Frequenz zu einem der Integrierer (11,12;13,14) zu liefern.

5. Filterschaltung nach Anspruch 4, dadurch gekennzeichnet, daß der Ausgangsanschluß der Integrierkapazität (12) des ersten Integrierers (11,12) mit einem Erdanschluß verbunden ist, und gekennzeichnet durch Mittel zum Verbinden des invertierenden Eingangsanschlusses des zweiten Integrierers (13,14) mit einem Erdanschluß, wobei die Eingangssignalliefermittel den nichtinvertierenden Eingangsanschluß des ersten Integrierers (11,12) verbinden, um das Eingangssignal mit einer konstanten Frequenz zu empfangen, wobei die Schaltmittel (18) angepaßt sind, um wahlweise den Ausgangsanschluß der Integrierkapazität (14) des zweiten Integrierers (13,14) mit dem nichtinvertierenden Eingangsanschluß des ersten Integrierers (11,12) oder mit dem Erdanschluß zu verbinden.

6. Filterschaltung nach Anspruch 4, dadurch gekennzeichnet, daß der invertierende Eingangsanschluß des zweiten Integrierers (13,14) mit der Integrierkapazität (12) des ersten Integrierers (11,12) verbunden ist, wobei die Schaltmittel (18) aus einer ersten Schalteinheit (18A) bestehen, die angepaßt sind, den nichtinvertierenden Eingangsanschluß des ersten Integrierers (11,12) mit dem Erdanschluß oder mit dem Eingangssignal mit der konstanten Frequenz zu verbinden, und aus einer zweiten Schalteinheit (18B), um wahlweise die Integrierkapazität (12) des ersten Integrierers (11,12) mit dem Erdanschluß oder mit dem Eingangssignal mit der konstanten Frequenz zu verbinden, wobei die erste und der zweite Schalteinheit (18A,18B) betätigt werden, solange die Schaltmittel (18) betätigt werden, um die Eingangssignale mit der konstanten Frequenz mit dem nichtinvertierenden Eingang des ersten Integrierers (11,12) und die Integrierkapazität (12) des ersten Integrierers (11,12) mit Erde zu verbinden.

7. Filterschaltung nach Anspruch 4, dadurch gekennzeichnet, daß die Integrierkapazität (12) des ersten Integrierers (11,12) mit dem Eingangssignal mit der konstanten Frequenz verbunden ist, wobei die Schaltmittel (15) eine Widerstandsschaltung (R_1,R_2,R_3) umfassen, die mit dem Ausgangsanschluß und dem invertierenden Eingangsanschluß des zweiten Integrierers (13,14) und mit der Integrierkapazität (12) des ersten Integrierers verbunden sind, wobei die Schalteinheit (SW) den Widerstandswert der Widerstandsschaltung (R_1,R_2,R_3) umschaltet.

8. Filterschaltung nach Anspruch 4, dadurch gekennzeichnet, daß der nichtinvertierende Eingangsanschluß des ersten Integrierers (11,12) mit dem Eingangssignal mit der konstanten Frequenz verbunden ist und wobei die Schaltmittel (15) eine Widerstandsschaltung (R_2,R_2,R_3) einschließen, die mit dem Ausgangsanschluß des zweiten Integrierers (13,14) und mit Erde verbunden ist, wobei die Schalteinheit (15) den Widerstandswert der Widerstandsschaltung (R_1,R_2,R_3) umschaltet.

9. Filterschaltung nach einem der Ansprüche 1 bis 8, dadurch gekennzeichnet, daß die Schaltmittel (18,15,SW) betätigt werden, um die Filtercharakteristik des Filters von einem Tiefpaßfilter in ein Sperrfilter während einer Justierung der Filterschaltung umzuschalten.

10. Filterschaltung nach einem der Ansprüche 1 bis 8, dadurch gekennzeichnet, daß die Schaltmittel (18,15,SW) betätigt werden, um die Filtercharakteristik des Filters von einem Bandpaßfilter in ein Sperrfilter während einer Justierung der Filterschaltung umzuschalten.

Revendications

1. Circuit de filtre comprenant :
deux intégrateurs (11, 12 ; 13, 14) dont chacun comporte un amplificateur (11 ; 13) et une capacité d'intégration (12 ; 14), une borne de sortie du premier desdits intégrateurs (11, 12) étant connectée à

une borne d'entrée d'un second desdits intégrateurs (13, 14), une borne de sortie dudit second intégrateur (13, 14) étant appliquée en retour à une borne d'entrée d'inversion dudit premier intégrateur (11, 12) et à une borne d'entrée d'inversion dudit second intégrateur (13, 14) via un circuit de retour (15) et la capacité d'intégration (12) dudit premier intégrateur (11, 12) étant connectée audit circuit de retour (15) ;

un moyen de commutation (18 ; SW, 15) connecté à au moins l'un desdits premier et second intégrateurs (11, 12 ; 13, 14) pour assurer la commutation des caractéristiques dudit circuit de filtre ; et

un moyen sensible à un signal de commande pour actionner sélectivement ledit moyen de commutation (18 ; SW, 15),

caractérisé en ce que :

la borne de sortie dudit premier intégrateur (11, 12) est connectée à l'entrée de non inversion dudit second intégrateur (13, 14) ;

la borne d'entrée de non inversion (Ta) du premier intégrateur (11, 12), le point de jonction (Tb) de ladite capacité d'intégration (12) dudit premier intégrateur, avec ledit circuit de retour (15), et une borne (Tc) de la capacité d'intégration (14) du second intégrateur (13, 14) se voient appliquer des signaux d'entrée ou sont respectivement mis à la masse pour former sélectivement différentes configurations de filtre ; et

ledit moyen de commutation (18 : SW, 15) est conçu pour faire commuter le circuit de filtre d'une première configuration de filtre à une seconde configuration de filtre pendant un réglage, ladite seconde configuration de filtre présentant une caractéristique de filtre qui est davantage distincte et qui convient donc mieux pour un réglage facile et précis que la caractéristique de filtre de ladite première configuration de filtre.

2. Circuit de filtre selon la revendication 1, caractérisé par un moyen sensible à un second signal de commande pour régler les caractéristiques dudit circuit de filtre tandis que ledit moyen de commutation (18, SW, 15) est actionné.

3. Circuit de filtre selon la revendication 1 ou 2, caractérisé en ce que ledit moyen de commutation inclut une unité de commutation (SW) destinée à commuter la valeur du Q dudit circuit de filtre, ladite unité de commutation (SW) étant commutée pour augmenter la valeur du Q pendant le réglage dudit circuit de filtre.

4. Circuit de filtre selon l'une quelconque des revendications 1 à 3, caractérisé par un moyen d'application d'entrée (16, SG) pour appliquer un signal d'entrée à fréquence constante à l'un desdits intégrateurs (11, 12 ; 13, 14).

5. Circuit de filtre selon la revendication 4, caractérisé en ce que la borne de sortie de la capacité d'intégration (12) dudit premier intégrateur (11, 12) est connectée à une borne de masse et caractérisé par un moyen pour connecter la borne d'entrée d'inversion dudit second intégrateur (13, 14) à une borne de masse, ledit moyen d'application connectant la borne d'entrée de non inversion dudit premier intégrateur (11, 12) pour recevoir ledit signal d'entrée à fréquence constante, ledit moyen de commutation (18) étant conçu pour connecter de façon sélective la borne de sortie de la capacité d'intégration (14) dudit second intégrateur (13, 14) à la borne d'entrée de non inversion dudit premier intégrateur (11, 12) ou à ladite borne de masse.

6. Circuit de filtre selon la revendication 4, caractérisé en ce que la borne d'entrée d'inversion dudit second intégrateur (13, 14) est connectée à la capacité d'intégration (12) dudit premier intégrateur (11, 12), ledit moyen de commutation (18) est constitué par une première unité de commutation (18A) conçue pour connecter sélectivement la borne d'entrée de non inversion dudit premier intégrateur (11, 12) à ladite borne de masse ou audit signal d'entrée à fréquence constante, et par une seconde unité de commutation (18B) pour connecter sélectivement la capacité d'intégration (12) dudit premier intégrateur (11, 12) à ladite borne de masse ou audit signal d'entrée à fréquence constante, lesdites première et seconde unités de commutation (18A, 18B) étant actionnées tandis que ledit moyen de commutation (18) est actionné pour connecter lesdits signaux d'entrée à fréquence constante à l'entrée de non inversion dudit premier intégrateur (11, 12) et pour connecter la capacité d'intégration (12) du premier intégrateur (11, 12) à la masse.

7. Circuit de titre selon la revendication 4, caractérisé en ce que la capacité d'intégration (12) dudit premier intégrateur (11, 12) est connectée audit signal d'entrée à fréquence constante, ledit moyen de commutation (15) incluant un circuit de résistance (R_1, R_2, R_3) connecté à la borne de sortie et à la borne d'entrée d'inversion dudit second intégrateur (13, 14) ainsi qu'à la capacité d'intégration (12) dudit premier intégrateur, ladite unité de commutation (SW) commutant la valeur de résistance dudit circuit de résistance (R_1, R_2, R_3).

8. Circuit de filtre selon la revendication 4, caractérisé en ce que la borne d'entrée de non inversion dudit premier intégrateur (11, 12) est connectée audit signal d'entrée à fréquence constante et ledit moyen de commutation (15) inclut un circuit de résistance (R_1, R_2, R_3) connecté à la borne de sortie dudit second intégrateur (13, 14) ainsi qu'à la masse, ladite unité de commutation (15) commutant la valeur de résistance dudit circuit de résistance (R_1, R_2, R_3).

9. Circuit de filtre selon l'une quelconque des revendications 1 à 8, caractérisé en ce que ledit moyen de commutation (18, 15, SW) est actionné pour commuter les caractéristiques de filtre dudit filtre d'un filtre passe-bas à un filtre du type bouchon pendant le réglage dudit circuit de filtre.

10. Circuit de filtre selon l'une quelconque des revendications 1 à 8, caractérisé en ce que ledit moyen de commutation (18, 15, SW) est actionné pour commuter les caractéristiques de filtre dudit filtre d'un filtre passe-bande à un filtre du type bouchon pendant le réglage dudit circuit de filtre.

FIG. 1

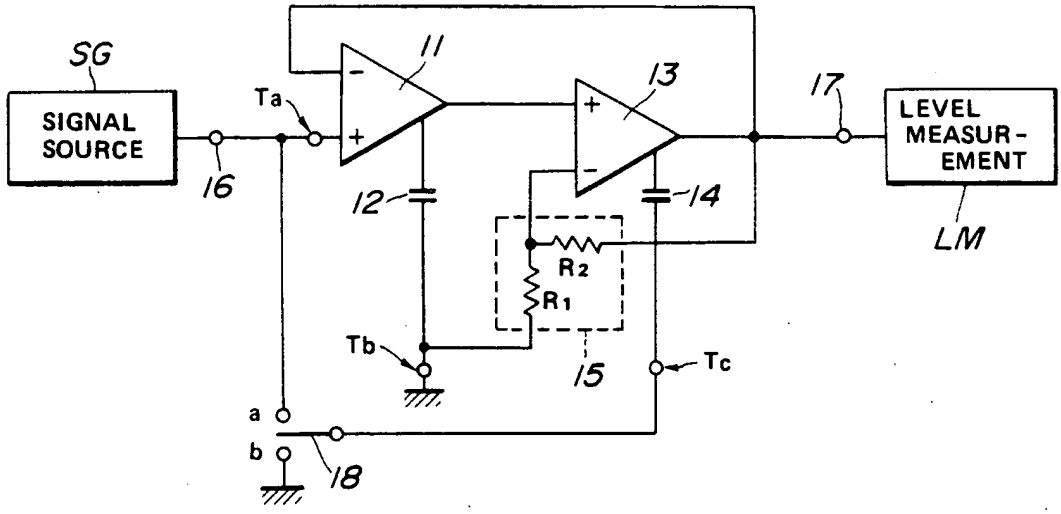
SG
SIGNAL SOURCE
16
Ta
11
12
13
14
17
LEVEL MEASUR-EMENT
LM
R2
R1
15
Tb
Tc
a
b
18

FIG. 2

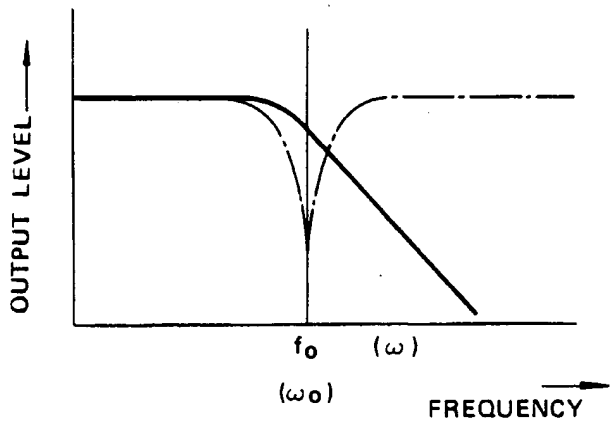
OUTPUT LEVEL
fo
(ω)
(ωo)
FREQUENCY

FIG.3

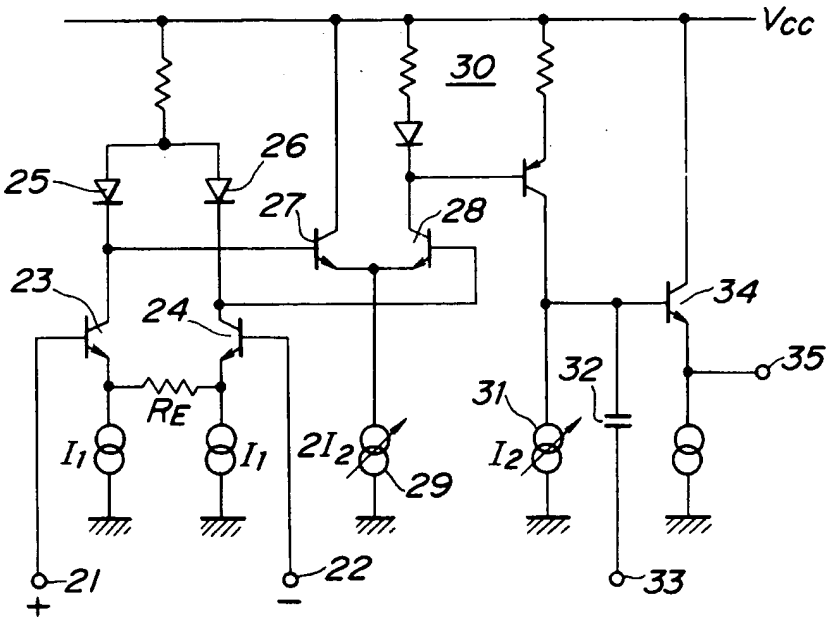

FIG.4

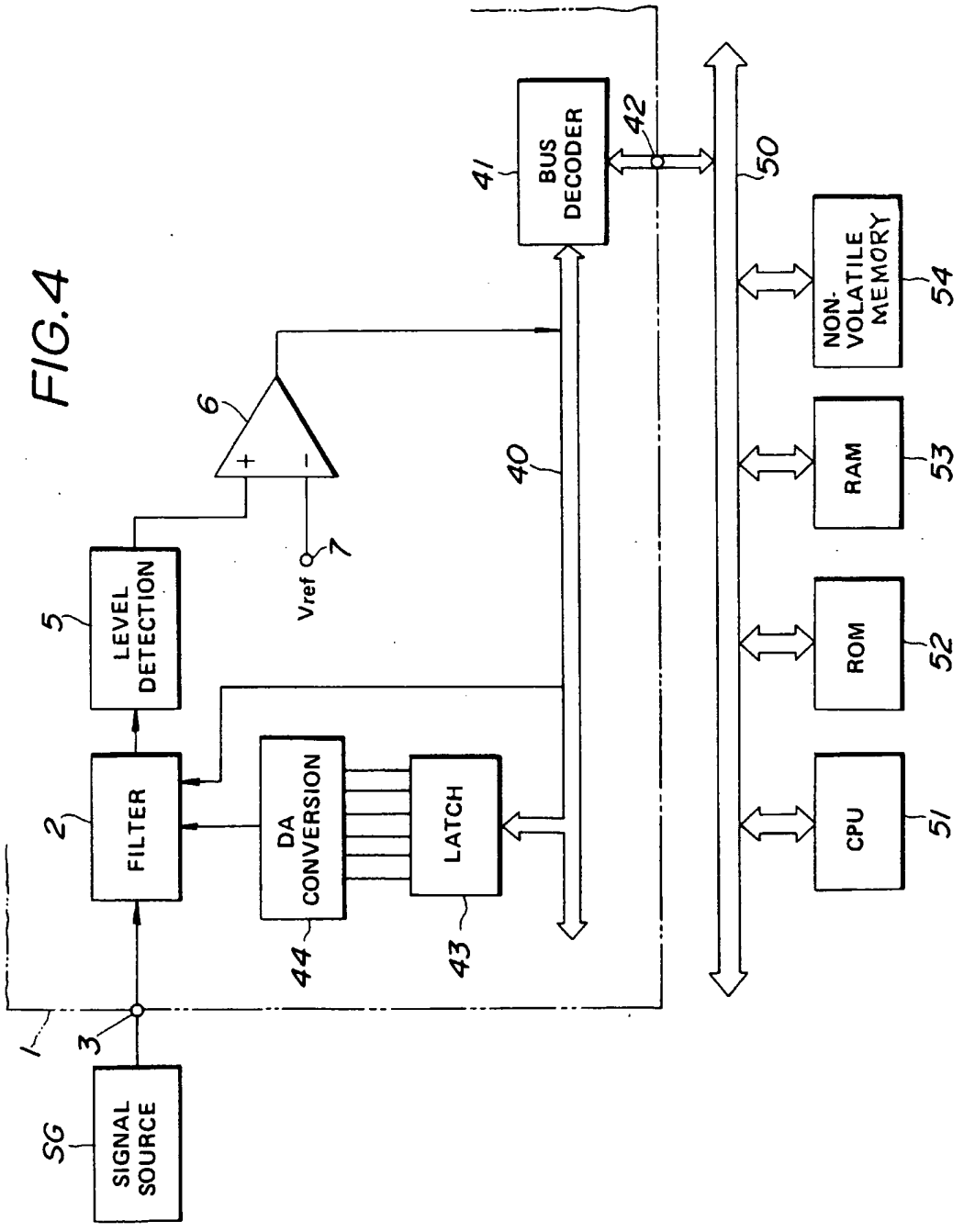
SIGNAL SOURCE
SG
1
3
FILTER
2
LEVEL DETECTION
5
6
+
-
Vref
7
DA CONVERSION
44
LATCH
43
40
BUS DECODER
41
42
50
NON-VOLATILE MEMORY
54
RAM
53
ROM
52
CPU
51

FIG.5

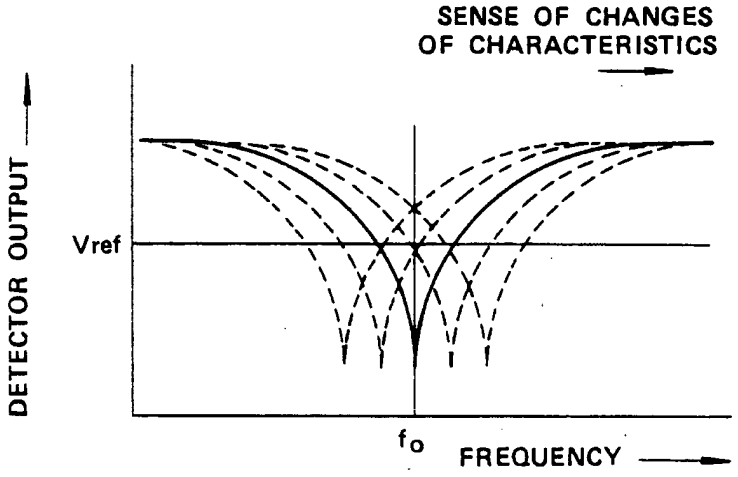
SENSE OF CHANGES
OF CHARACTERISTICS
DETECTOR OUTPUT
Vref
fo
FREQUENCY

FIG.6

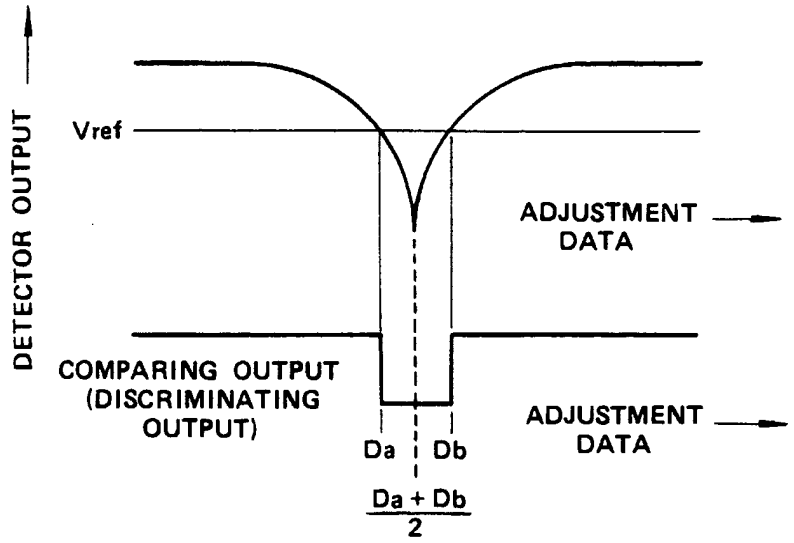
DETECTOR OUTPUT
Vref
ADJUSTMENT
DATA
COMPARING OUTPUT
(DISCRIMINATING
OUTPUT)
ADJUSTMENT
DATA
Da
Db
Da + Db
2

FIG.7

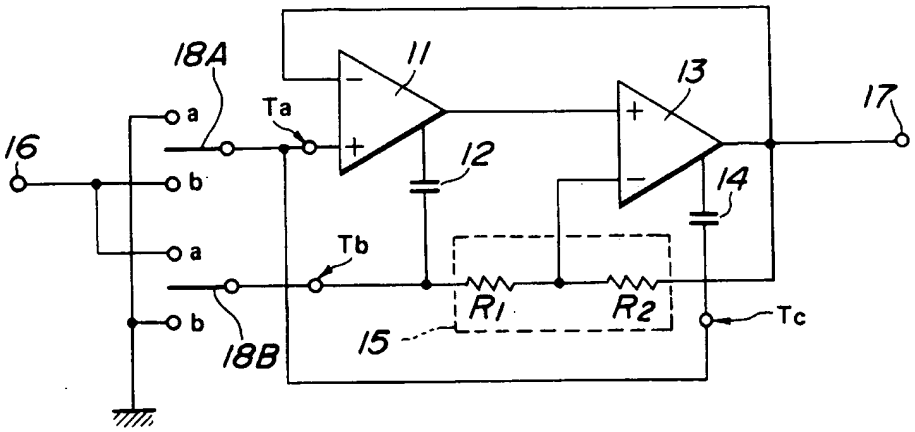
18A
11
13
17
16
a
Ta
12
b
14
a
Tb
b
R1
R2
Tc
15
18B

FIG.8

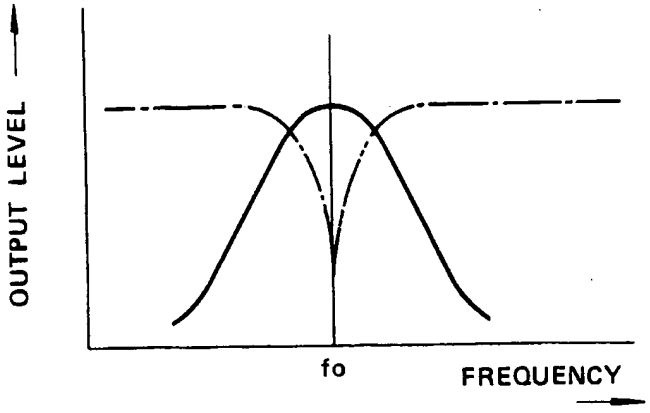
OUTPUT LEVEL
fo
FREQUENCY

FIG. 9

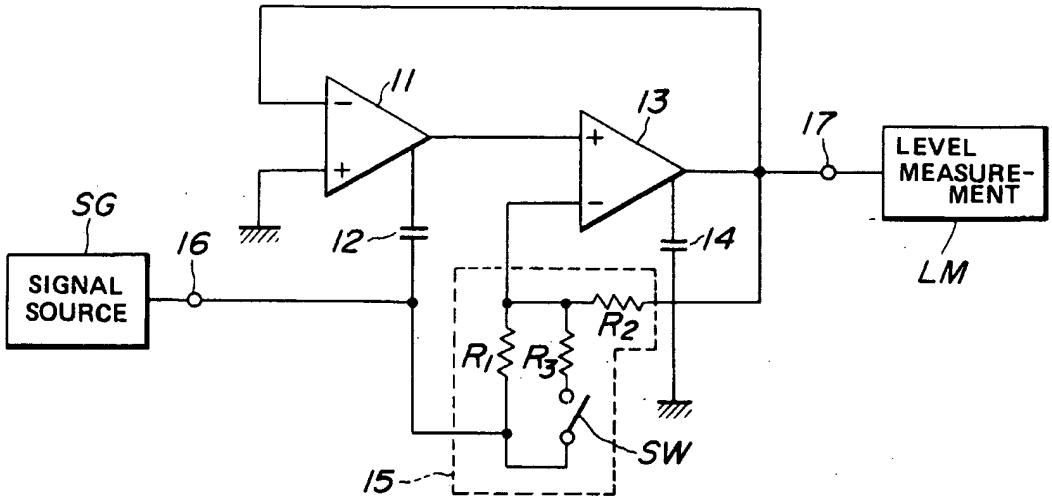
11
13
17
LEVEL MEASURE-MENT
LM
SG
SIGNAL SOURCE
16
12
14
R2
R1
R3
SW
15

FIG. 10

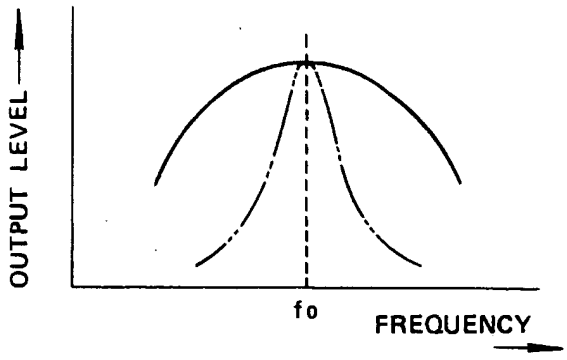
OUTPUT LEVEL
fo
FREQUENCY

FIG. 11

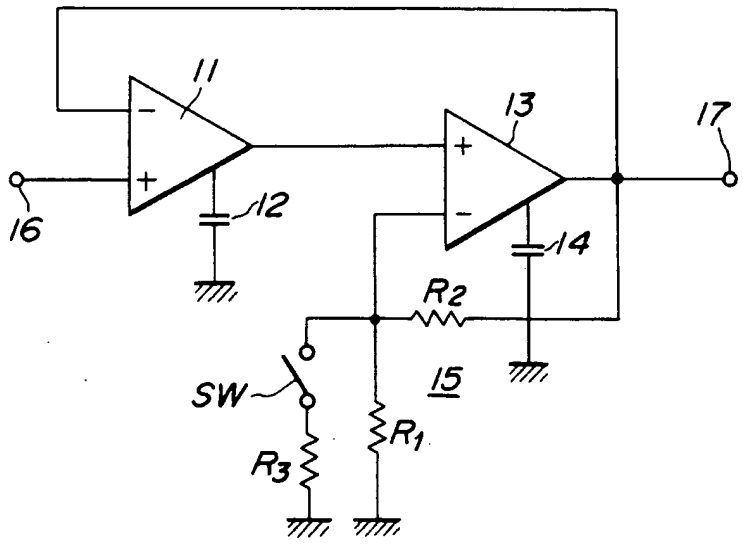

FIG. 12